REMARKS:

Claim Rejections Under 35 USC 102:

Claims 1-9 were rejected under 35 USC 102(b) as being anticipated by Kusonoki, (US 6,066,880). Further, claims 1-7 were rejected under 35 USC 102(b) as being anticipated by Shigyo (JP 7-273212). Claim 1 was also rejected under 35 USC 102(e) an being anticipated by Rotondoro (US PG-Pub No. 20002/0058424).

Applicants have amended claim 1 to clarify the distinctions between the invention recited in the claims and the cited prior art references. Support for the amendment to claim 1 may be found at page 10, line 13 through page 11, line 11 in the specification.

The Examiner rejected claims 1-9, indicating that Kusonoki at FIGS. 68-79; col. 3, lines 5-42; and col. 7, lines 60-65 disclosed all of the elements of claims 1-9. Applicant has now amended claim 1 to include the limitation that the depth of the peak concentration of the buried channel implant is at a selected level in the substrate below the insulating gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer. Kusonoki does not teach or suggest this limitation. At best, Kusonoki shows a conventional buried channel without any teachings as to concentrations of the implant or selection of the position of the buried channel.

For similar reasons, Rotondaro fails to teach or suggest all of the elements of claim 1. Rotondaro teaches in the background the conventional operation of a MOS transistor in the enhancement mode. Zone 80 is not a buried channel but instead is described as an inversion region. Thus, Rotondar fails to teach or suggest all of the elements of claim 1, including a buried channel or the positioning of a buried channel.

Finally, Shigyo in the abstract and drawings shows n type embedded layer in a p-well, but at he cited location doesn't teach or suggest limitations as to operating conditions (such as biasing), concentrations of the implant, or positioning of the embedded layer relative to a selected effective gate dielectric value. Thus, for at least these reasons, Shigyo fails to teach or suggest the limitations of claim 1. Claims 2-9 are dependant claims, and submitted to be allowable at least due to these dependencies.

Claim 22 is new and depends from claim 1. It is submitted to be allowable at least due to this dependency. Support for this claim may be found in the specification at page 9, lines 20-27.

Claim 23 is also new and in independent form. Support for these amendments may be found in the specification page 10, line 22 through page 11, line 11 and in FIGS. 1-10b. It is submitted to be allowable over the cited prior art references for at least the reason that none of the cited references teaches or suggests an integrated circuit having a first device with a first effective gate dielectric value, and a second device having a second and greater gate dielectric value, the second value resulting form a combination of the gate dielectric and a depleted zone between the interface and the buried channel and for the reasons discussed above with respect to claim 1. For example, Rotundaro in the background refers to a single conventional MOS device. Similarly, there is no teaching or suggestion in Kusonoki and Shigyo as to multiple gate dielectric thicknesses achieved by buried channels. For at least these reasons, applicants submit that new claims 23-26 are allowable, the latter claims being dependant from claim 23.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. If any fees are due over and above the fees provided with the amendment, such fees may be charged to deposit account No. 12-2252 (client docket 01-721).

Respectfully submitted,
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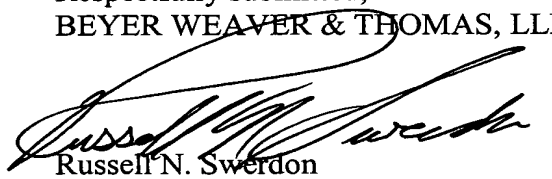

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APPENDIX

Version of amended claims showing the changes made

1. (Once Amended) In a semiconductor device having at least an insulating gate dielectric layer and a gate fabricated upon a semiconductor substrate, a buried channel implanted below the insulating gate dielectric layer, the buried channel being doped with a predetermined dopant and a peak concentration of the dopant positioned at a selected level in the substrate below the insulating gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer so that when the gate is biased with respect to the substrate, the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer.

22. (new) The semiconductor device of claim 1, wherein the insulating gate dielectric layer and the substrate forms an interface and the peak concentration of implanted dopants in the buried channel is located between 400 and 1000 Angstroms below the interface.

23. (new) An integrated circuit fabricated on a semiconductor substrate and having at least two devices, each of the devices having a different effective gate oxide thickness, the circuit comprising:

a first device having a gate disposed on a gate dielectric layer, the gate dielectric layer having a first thickness and a first effective gate dielectric value and disposed on the semiconductor substrate;

a second device having a gate disposed on a gate dielectric layer having the first thickness and the first effective gate dielectric value, the gate dielectric layer fabricated on a semiconductor substrate, a buried channel implanted below the gate dielectric layer, the buried channel being doped with a predetermined dopant and a peak concentration of the dopant positioned at a selected level in the substrate below the gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer to increase the effective gate dielectric thickness of the second device, wherein the level is selected so that the effective gate dielectric thickness of the second device is a predetermined value greater than the first effective gate dielectric value.

24. (new) The integrated circuit as recited in claim 23 wherein the insulating gate dielectric layer and the substrate forms an interface and the peak concentration of implanted dopants in the buried channel is located between 400 and 1000 Angstroms below the interface.

25. (new) The integrated circuit as recited in claim 23 wherein the device is a MOS capacitor.

26. (new) The integrated circuit as recited in claim 23 wherein the substrate is a p-type substrate and the buried channel is an n-type buried channel.